

“Load Characterization and Matching of High–Power RF Amplifiers”

Richard W. Brounley, P.E

Introduction and Statement of Purpose of Paper

Many applications for RF Power Amplifiers (RFPA's) require that they operate into Voltage Standing Wave Ratio's (VSWR's) from 1:1 to 50:1. It is important to characterize the RFPA in such a manner as to understand it's performance regarding stability, dissipation, efficiency, voltage breakdown, and power developed into mismatched loads. Some representative applications are for driving lasers, plasma chambers and ICP torches.

This paper describes the techniques used to characterize an RFPA along with results obtained on a 45 MHz single output transistor model. A multiple transistor RFPA at 80 MHz used as a laser driver with a power output of 1200 watts peak is described. Protection methods, matching circuits and components available for high power are also discussed. The paper applies primarily to saturated amplifiers operating in class C, D, or E and capable of efficiencies in excess of 70%.

45 MHz Test Model

Figure 2 shows the schematic diagram of a 45 MHz final amplifier stage selected as a test model. This frequency was chosen because the transistor is capable of sustaining harmonics up to at least the fifth thereby generating a drain waveform consistent with a high-efficiency amplifier. The drain waveforms and frequency spectrum are shown in the pictures of *Figures 12, 13 and 14* and will be discussed in more detail later. The tests results of the model are shown in *Figure 2*. The input and output circuits use a two-step matching circuit to transform the low input and output impedances to 50 ohms. This matching method is better than a single step match because it's broader in bandwidth and the components are less critical. The gate voltage is used to switch the amplifier on and off when used in the pulsed mode as with a laser driver.

In order to gain insight into the mismatched performance of the amplifier, a model using a voltage generator in series with a source resistance (R_s) and a load impedance (Z_l) is shown in *Figure 3*. *Figure 4* shows the manner in which the efficiency of an amplifier, simulated by the model, varies with the source resistance. The efficiency of an amplifier with a load resistance of 50 ohms and a source resistance of 20 ohms is about 72% and is used to represent the high-efficiency amplifier for analysis. While the model is relatively simple, it gives remarkable insight into the characterization when compared with the actual test results. A more rigorous analysis would be a worthwhile project.

Figure 3 gives the equation for the series load impedance Z_l in terms of the reflection coefficient $p < 0$. Z_l can then be found for different VSWR's as the

phase angle is varied around the Smith Chart. From this the power developed (P_o) can then be calculated as shown by the equation. *Figure 5* shows the manner in which the power varies for different source resistances for a VSWR of 2:1 ($\rho = .33$). A constant voltage of 180 volts and a source resistance of 20 ohms are used for the calculations because, when used in the model, they result in a power output of 330 watts and an efficiency of 72%. This is close to the super-pulse test results shown in *Figure 2*.

Notice how the developed power varies as the phase angle and source resistance are varied. For a 50-ohm source resistance, the power is flat versus the phase angle. As the source resistance is decreased, the power increases and is maximum at $\theta = 180$ degrees. This is true provided the generator has a constant voltage and source resistance. For the assumed source resistance of 20 ohms, the power increases to 410 ohms where $\theta = 180$ degrees and is greater than the 330 watts developed into a 50-ohm load. The characterization has been done for other VSWR's of 3:1, 4.9:1, and 9.5:1 and are discussed later.

In order to be able to compare the calculated characteristics with the test model of *Figure 2*, a test is conducted as shown in *Figure 6*. The test amplifier is operated in the pulsed mode at a pulse width of 200 usec at a duty cycle of 10%. This enables the transistor to survive any mismatched condition without failure. Mismatches are placed ahead of the 50-ohm measuring system and the phase of the mismatch varied using 15-degree lengths of coaxial cable. The power is measured using a peak reading power meter. The test results are shown in *Figure 7*.

Figures 8, 9, 10, 11 show how the calculated and measured data compare. It should be remembered in examining the curves, that a linear constant voltage generator was assumed along with a constant source resistance. The curves show that the tested amplifier follows the general shape of the calculated curves even though there is some error in the absolute values. The tested amplifier shows deviation from the calculated curve particularly for the 9.5:1 VSWR when the phase angle approaches 180 degrees. This is probably because the transistor cannot support the necessary current and the model no longer represents the transistor's operation.

Transistor Drain Voltage Characteristics

The drain voltage waveforms of a transistor operating in one of the high efficiency classes of operation (C, D, or E) demonstrate voltages in excess of twice the $B+$ voltage. *Figure 12* shows a photograph of the drain voltage of the test amplifier into a 50-ohm load. The peak drain voltage is 160 volts, which is 3.33 times $B+$. *Figure 13* shows a photograph of the frequency spectrum of the drain voltage connected to a Spectrum Analyzer using a capacitive probe where it is shown to support harmonics out to the seventh and beyond. *Figure 14* is a photograph of the drain voltage when the amplifier is operated into a 65:1 VSWR at the phase angle that generates the maximum peak drain voltage. This voltage excursion is 200 v or about four times $B+$. When it is considered that the transistor is rated by the manufacturer at only 120 volts, the possibility of breakdown exists. Even so, transistors are consistently used in

this manner. The peak drain voltage swing comes from energy stored in the resonant circuit after the transistor has turned off. It has been observed in transformer coupled push-pull pairs, that this peak drain voltage swing can be as much as 5 or 6 times $B+$ when the amplifier is operated into high VSWR's. The peak drain voltage swing comes from the opposite transistor as it turns on and comes from a different source than the single ended circuit in the test model.

In order for the amplifier to withstand these peak voltages without failure, a term Transient VSWR performance has been coined. The VSWR test described previously is used to insure that the transistors are capable of withstanding this stress. It has been found that some manufacturers transistors are more rugged and will pass this test consistently while others are less reliable. There is no protection method that is fast enough to protect from this type of failure and transistor manufacturers do not specify their transistors to operate in this manner. The alternative would be to reduce the $B+$ to about 30 volts thereby reducing the peak power capability to 40%. This would be a major cost disadvantage and the Transient VSWR test has proven effective in producing reliable amplifiers without reducing the $B+$.

VSWR Power Dissipation Characterization

An amplifier's ability to operate reliably into a VSWR during its maximum average power output, is also part of the characterization procedure. The test procedure of *Figure 6* is repeated into a VSWR of 2:1 at a duty cycle of 40% while reading the peak or average power as well as the DC current. The dissipation in the transistor can then be calculated and plotted on a graph as shown in *Figure 15*. Knowing the transistor's thermal resistance and the operating case temperature, it can be determined if the transistor is within reliable dissipation limits. A junction temperature of 140 degrees C is considered to be a safe margin. The maximum dissipation for this transistor is 150 watts with a heatsink that limits the case temperature to 50 degrees C.

Protection Methods

When the amplifier shown in *Figure 2* exceeds the dissipation limit shown in *Figure 15*, a protection circuit must be activated to prevent possible failure. *Figure 16* is a photograph of the detected output power for a pulse length of 200 usec when the amplifier is operated into a 65:1 VSWR at a phase angle that causes maximum dissipation. The duty cycle is less than 10% so as not to be a factor. The droop in the detected output is caused by the transistor's junction heating. If the pulse were to be made longer, the transistor could fail. The protection circuit must react quickly enough to prevent this from occurring. Two methods of protection have been developed and are discussed in the following sections.

The first protection method is used primarily for RF laser drivers. Protection in a laser driver must retain the full peak power instead of folding back the RF output otherwise the laser will not strike. Lasers are usually difficult to strike when left off for a period of time and a pulsed format at full peak power acts like an automatic start-up circuit. Once the laser strikes and is correctly matched, the protection circuit is automatically disconnected. This method of protection limits the maximum pulse width and duty cycle when activated and is shown in *Figure 17* for the cw case. The maximum pulse width is limited to 200 usec and the duty cycle is limited to 10%. Under these conditions, the transistors in the output stage can survive any VSWR at any phase angle of the reflection coefficient. For this protection to be effective, the transistors must be free from self-oscillations between pulses.

In *Figure 17*, a VSWR comparator changes state when the reflected voltage exceeds the forward voltage at a predetermined VSWR set point. For the test amplifier described, this set point is for a VSWR of 2:1. The output of the comparator is connected to AND gate A. The other input to AND gate A is connected to a 200 usec one-shot generator. AND gate B is connected to the TTL input signal that is used to turn the RF generator on and off in accordance with the desired modulation of the laser. When a TTL signal is applied, the 200 usec one-shot is activated and inhibits AND gate A from sampling the output of the VSWR comparator. At the end of the 200 usec pulse, the comparator's output can be sampled. If it's high, indicating that protection is needed, the output of AND gate A activates a 2 msec one-shot. This 2 msec one-shot in turn disconnects AND gate B from the bias that controls the gate voltage on the

RF transistors. Should the comparator output remain low no protection is initiated. The waveform for cw protection is shown as a 200 usec pulse at a 10% duty cycle. For pulsed operation additional circuitry is required but is not covered here.

The second method of protection folds the RF output back in proportion to the magnitude of the VSWR. It is used for RF generators that excite plasma chambers or ICP torches. Referring to *Figure 18*, the output power of the RF generator is controlled by the B+ output of a switching regulator. A 0-10 volt control voltage is connected to the + input of operational amplifier A. The - input to the operational amplifier is connected to the output of operational amplifier B that samples the forward and reflected voltages from a directional coupler at its inputs. Operational amplifier C's + input is connected to the output from operational amplifier A. Its - input is connected to the forward output of the directional coupler. The output of operational amplifier C controls the reference voltage of the switching power supply and therefore the B+ voltage for the RF amplifiers. The forward voltage from the directional coupler is thereby compared with the 0-10 volt input and any error between the two is corrected by the amount of feedback. 20 db of feedback will reduce the error by a factor of 10:1.

When the reflected voltage exceeds the set point forward voltage, the output of operational amplifier B connected to the - input of operational amplifier A begins to control the B+ output thereby folding back the power in accordance with the magnitude of the VSWR. The gain of the fold-back loop determines the steepness of the fold-back curve shown in *Figure 18*. It needs to be steep

enough so that the dissipation in the transistors is below the maximum allowed but no steeper than necessary in order to generate the maximum allowable mismatched power for the chamber or torch. The speed of response needs to be greater than 500 usec in order to adequately protect the transistors.

A 1200 Watt Peak 80 MHz Laser Driver

Figure 19 is block diagram of a 1200-watt peak laser driver at a frequency of 80 Mhz. Two push-pull pairs are combined at the output using broadband transformer combiners. Emphasis is placed on stable performance into high VSWR's since high power lasers have low losses in their resonant structure and can be difficult to strike and match. The laser can have a VSWR as high as 50:1 before striking and the RF driver must generate maximum voltage into this mismatch. *Figure 20* is the VSWR characterization curves for this laser driver. The laser and RF driver are integrated by rotating the laser's unlit reflection coefficient phase angle back to the RF laser driver to match the maximum generated power output shown by the curves. This angle is about + 160 degrees and would require a 50-ohm cable 50 degrees long for best striking and pulsed characteristics if the unlit reflection coefficient of the laser is -100 degrees.

Matching Circuits and High Power Components

Matching circuits are an important part of the design of high-power RF amplifiers. A number of different types are discussed in the following sections along with components capable of withstanding the voltage and current stresses encountered.

Transmission Line Matching

Figure 21A through *C* show a number of matching methods classified as transmission line transformers.

1. *Figure 21A #1* is a quarter-wave transformer whose Characteristic Impedance (Z_0) equals the square root of the product of $Z_{in} \times Z_L$.
2. *Figure 21A #2* is a quarter-wave transmission line used as a balanced to unbalanced transformer or balun.
3. *Figure 21B #1* is a transmission line used as a balun but loaded with ferrite cores to reduce the length. The choking reactance should be at least $4 \times Z_0$ in order to present a high impedance to common mode currents and thereby preserve the balanced to unbalanced properties.
4. *Figure 21B #2* is a ferrite loaded unbalanced to unbalanced 4:1 transformer known as an unun. Z_0 equals $Z_L/2$ and the choking reactance should be at least $4 \times Z_0$.
5. *Figure 21C #1* is a high-power transformer using two coaxial cables wound on a common ferrite core that has a 4:1 impedance transformation. The cores

are connected as shown. The power capability is 1KW and its frequency response is 5- 100 Mhz. A separate balun is used to provide the balanced to unbalanced function. Z_o of the two coaxial cables is $Z_l/2$.

6. *Figure 21C #2* is actually not of the transmission line class but is included for discussion. A single turn primary uses brass tubes that are loaded with ferrite torroids. A secondary is passed through the tubes and the impedance transformation varies as N^2 where N is the number of turns. This is a popular selection because of its simplicity, but is limited in bandwidth and power. The bandwidth can be extended if the secondary is made to be an unum as shown in *Figure 21B #2* using a semi-rigid coaxial cable. The outer conductor is insulated and placed in side of the brass tubes. The brass tubes and semi-rigid outer conductor then become a 1:1 transformer with close coupling and also provide the isolation requirements. This arrangement has been called a tri-axial transformer and can extend the frequency response substantially.

LC Matching Circuits

Figures 22A and B show various forms of LC matching circuits. The equations for calculating the matching components are included.

1. *Figure 22A #1* transforms R_l to a higher input R_{in} using either a series L and a shunt C or series C and shunt L.
2. *Figure 22A #2* transforms R_l to a lower input R_{in} using either a shunt C and series L or a shunt L and series C.

3. *Figure 22B #1* is a pi match that can match either a higher or lower input resistance. The pi can either be a high pass or low pass version. The low pass is a lumped constant version of a quarter wave transmission line. The inductance and capacitance values are equal to the square root of the product of $R_{in} \times R_l$.

4. *Figure 22B #2* is the design of a high power pi match with a 10:1 ratio between R_l and R_{in} . The component values, current and voltages have been calculated and the performance tabulated. The output voltage lags the input by 90 degrees and acts like a quarter wave transmission line transformer.

A High Power Pin Diode Switch

Figure 23 is the schematic diagram of a high power pin diode switch used to switch a 220 pF ATC100E porcelain chip capacitor across a 50-ohm line for matching applications. The pin diode is a MA4PK3003 that has a breakdown voltage of 3000 volts, a series resistance of .25 ohms, and a power dissipation of 50 watts. The 220 pF chip capacitor has a breakdown rating of 3600 volts and a current rating of 10 amps. A Field Effect Transistor with a breakdown voltage of 900 volts is used to switch the pin diode on and off. A 450 volt DC voltage is used to back bias the diode in the off position. Switching speed is on the order of 10 usec. An opto-isolator connects the input to the switching circuit.

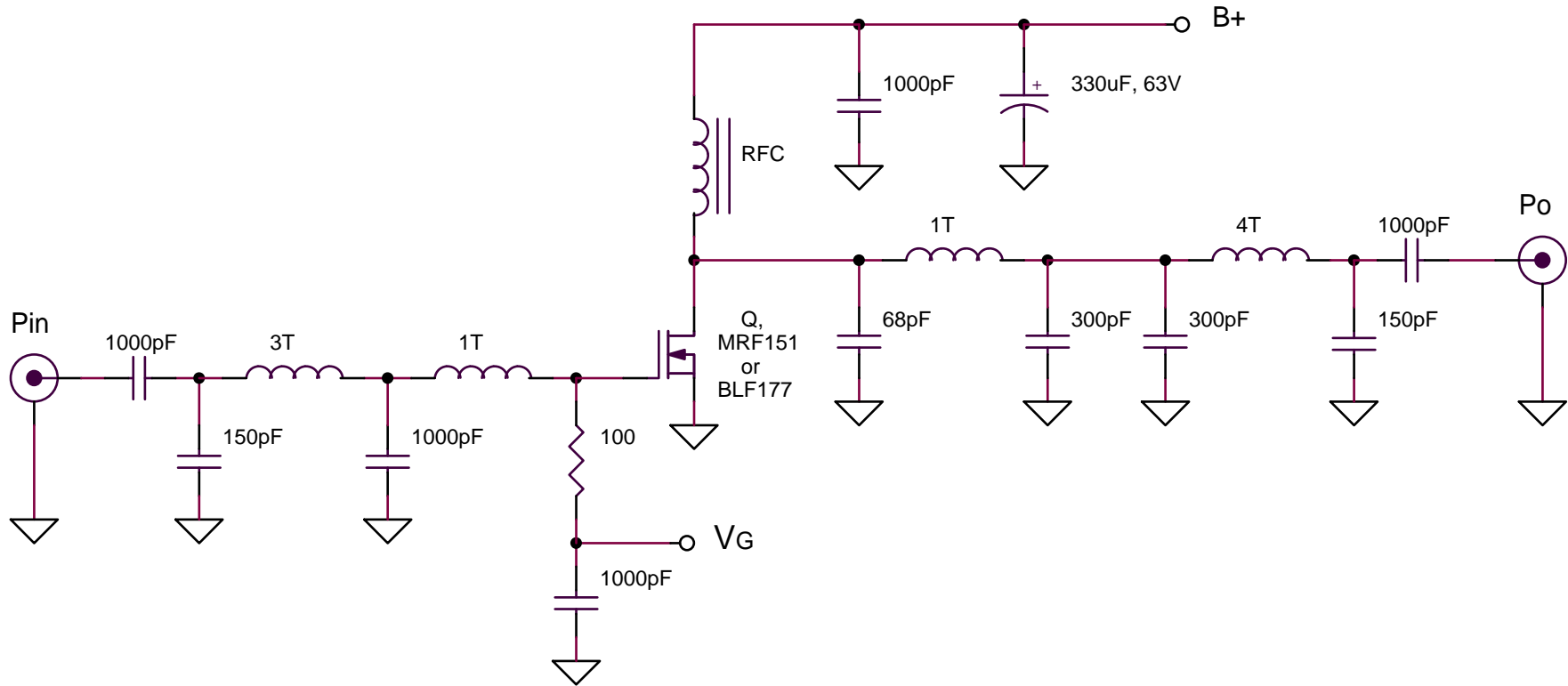
Summary

This paper has demonstrated that high-efficiency amplifiers can be characterized for their ability to drive mismatched loads. Such characterization data is important for applications such as lasers, plasma chambers, ICP torches and others. The drain voltage excursions have been shown to be three to five times the B+ voltage under mismatched conditions and amplifiers need to be tested in order to prevent failures. Methods of testing and protection under mismatched conditions have been presented. A summary of various matching circuits and high-power components has also been discussed.

The characterization analysis was based on a simple voltage generator model to demonstrate the amplifier's mismatched performance, but a more rigorous investigation would be a worthwhile project.

45.0 MHz Test Model Final Amplifier Schematic Diagram

Figure 2



45.0 MHz Test Performance

SuperPulse Mode:

B+	48 V
Po	350 WPK
Max. Duty Cycle	40%
Efficiency	74%
VSWR	2:1 (max. before protection)
Harmonics	> 30 dBc
Gain	20 dB

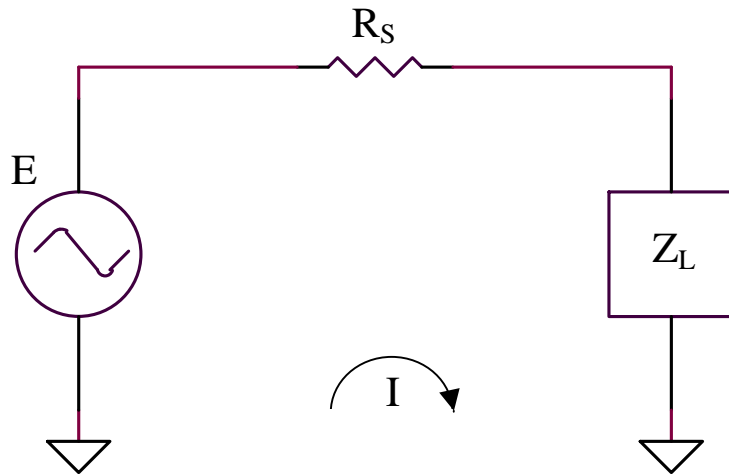
CW Mode:

B+	32 V
Po	165 W

Efficiency	82%
VSWR	2:1 (max. before protection)
Harmonics	> 30 dBc
Gain	17 dB

Equivalent Circuit Model

Figure 3



E is constant voltage source.

R_S is internal source impedance assumed constant.

Equations:

$$1. \quad Z_L = \left[\frac{\rho \angle \theta^\circ + 1}{1 - \rho \angle \theta^\circ} \right] \times 50$$

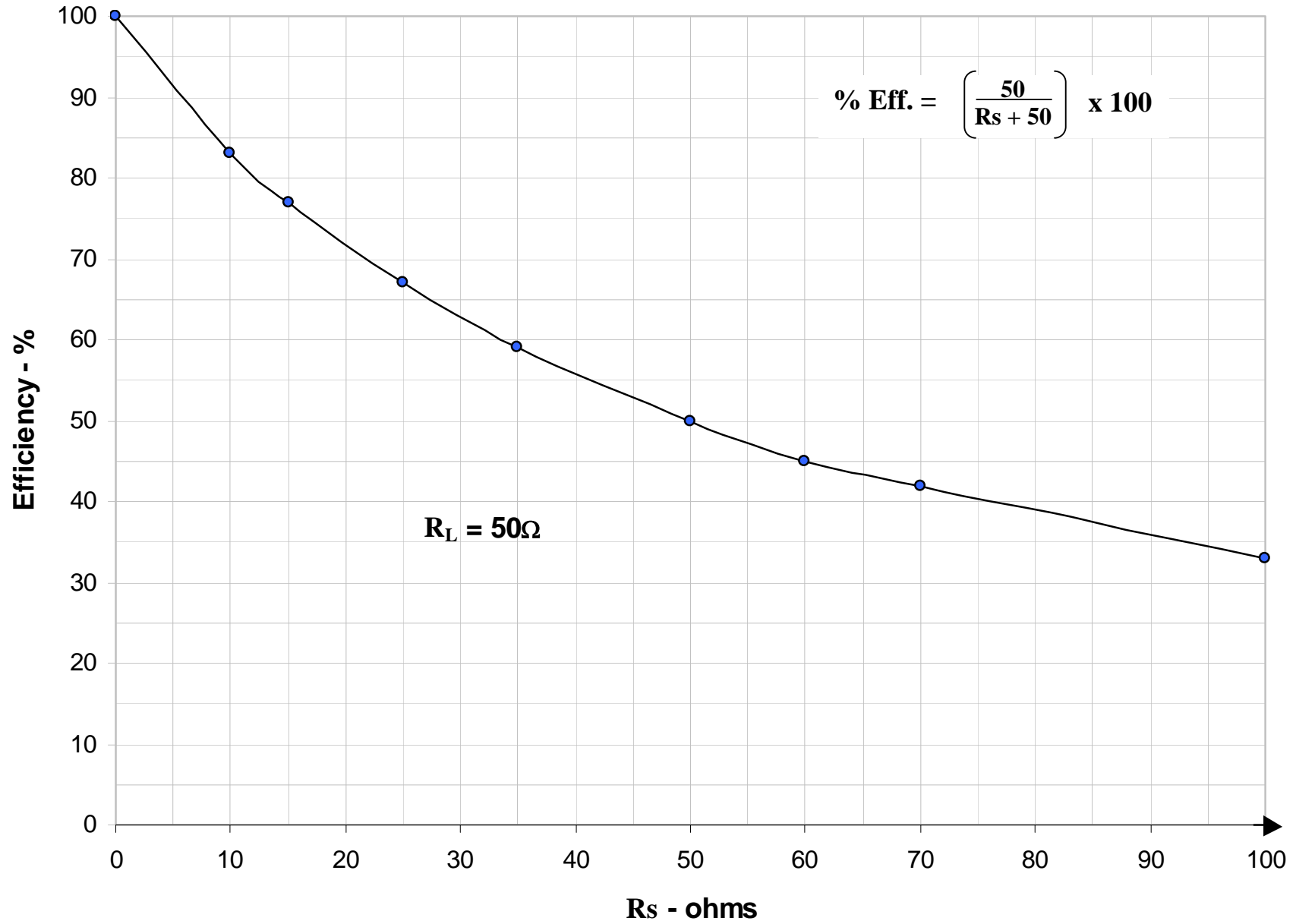
$\rho \angle \theta^\circ$ is reflection coefficient

Z_L is series equivalent transmission line impedance $R_L \pm j X_L$

$$2. \quad P_o = \left[\frac{E}{R_S + Z_L} \right]^2 \times R_L$$

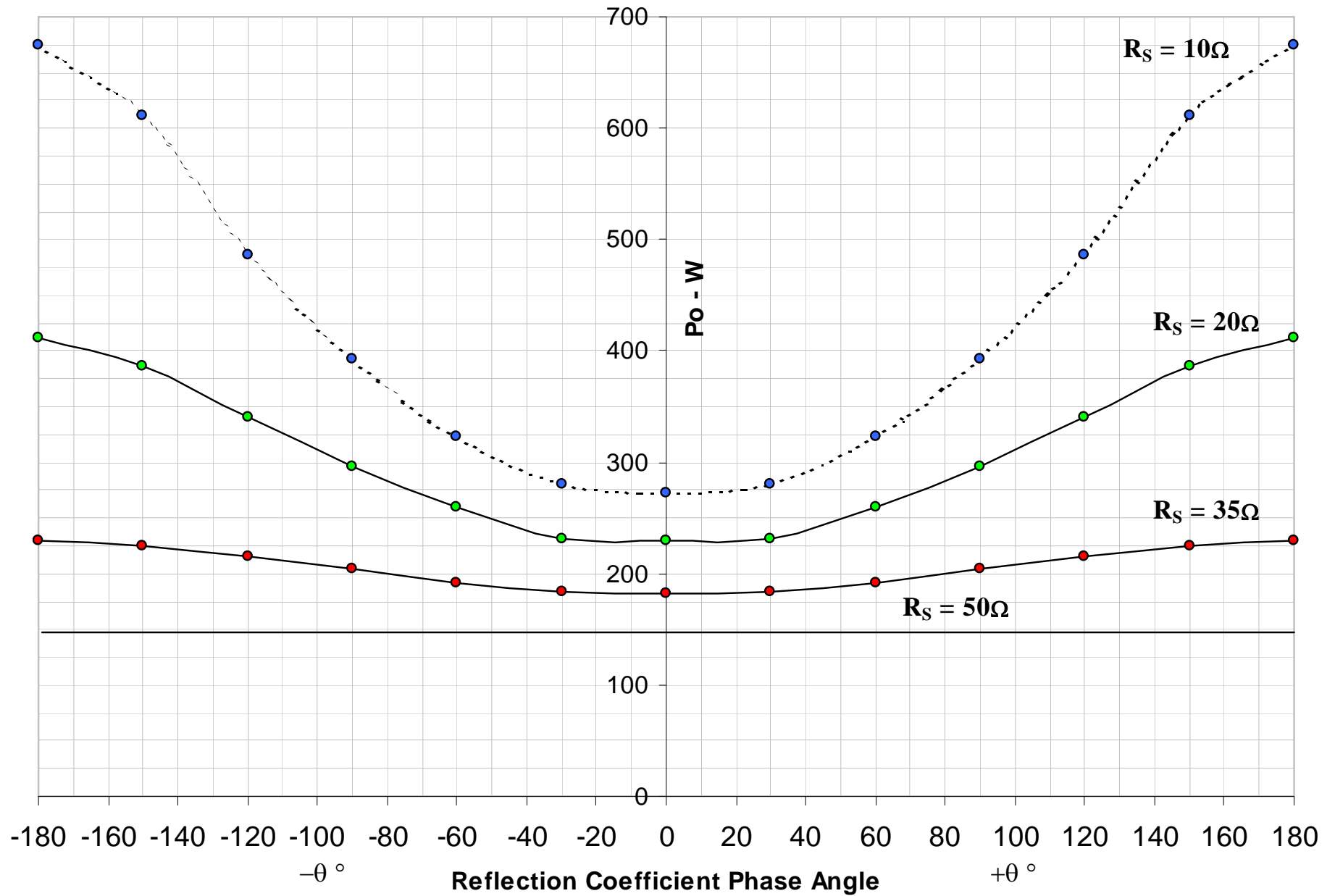
Equivalent Circuit Model Efficiency vs. R_S

Figure 4



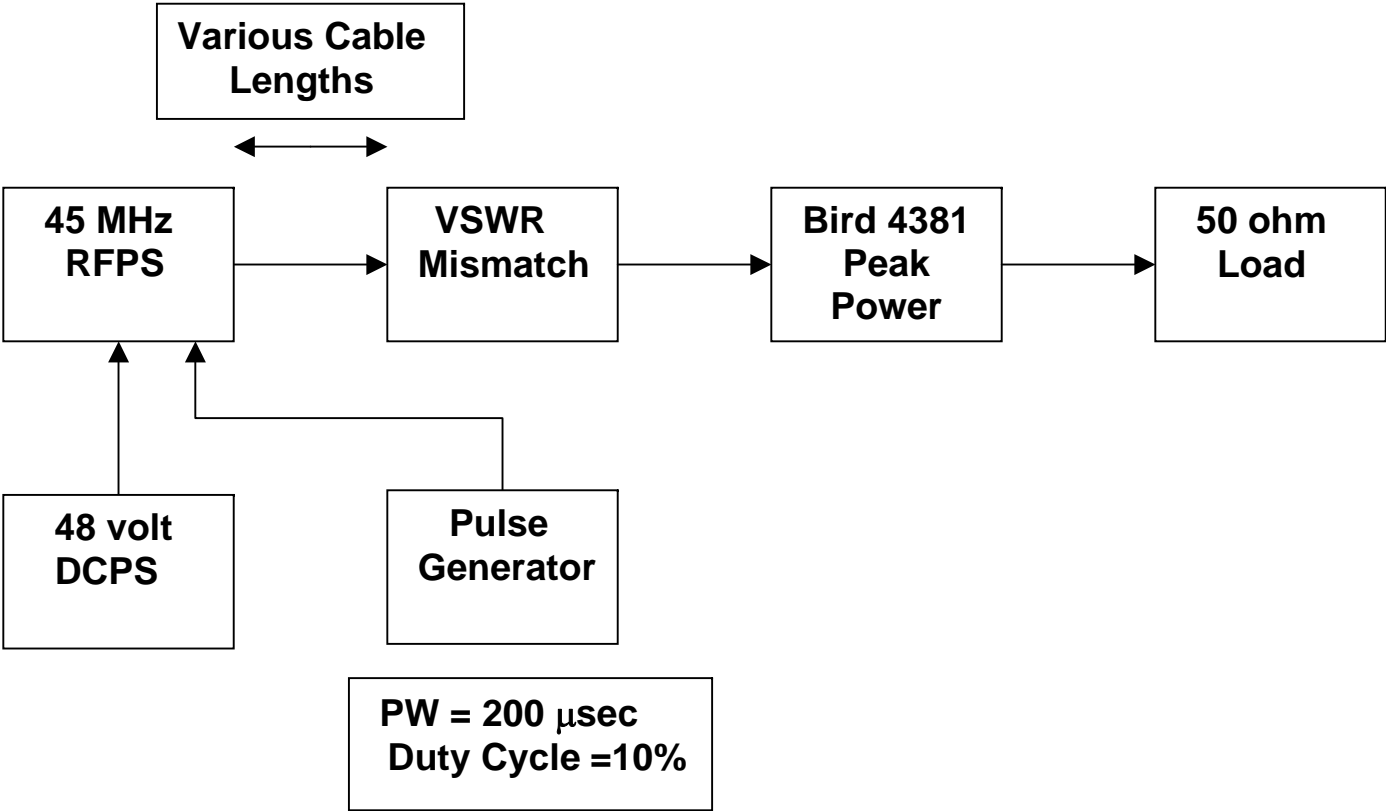
Calculated P_0 vs. θ for $\rho = .33$ and $R_S = 50\Omega, 35\Omega, 20\Omega, 10\Omega$

Figure 5



VSWR Test Arrangement

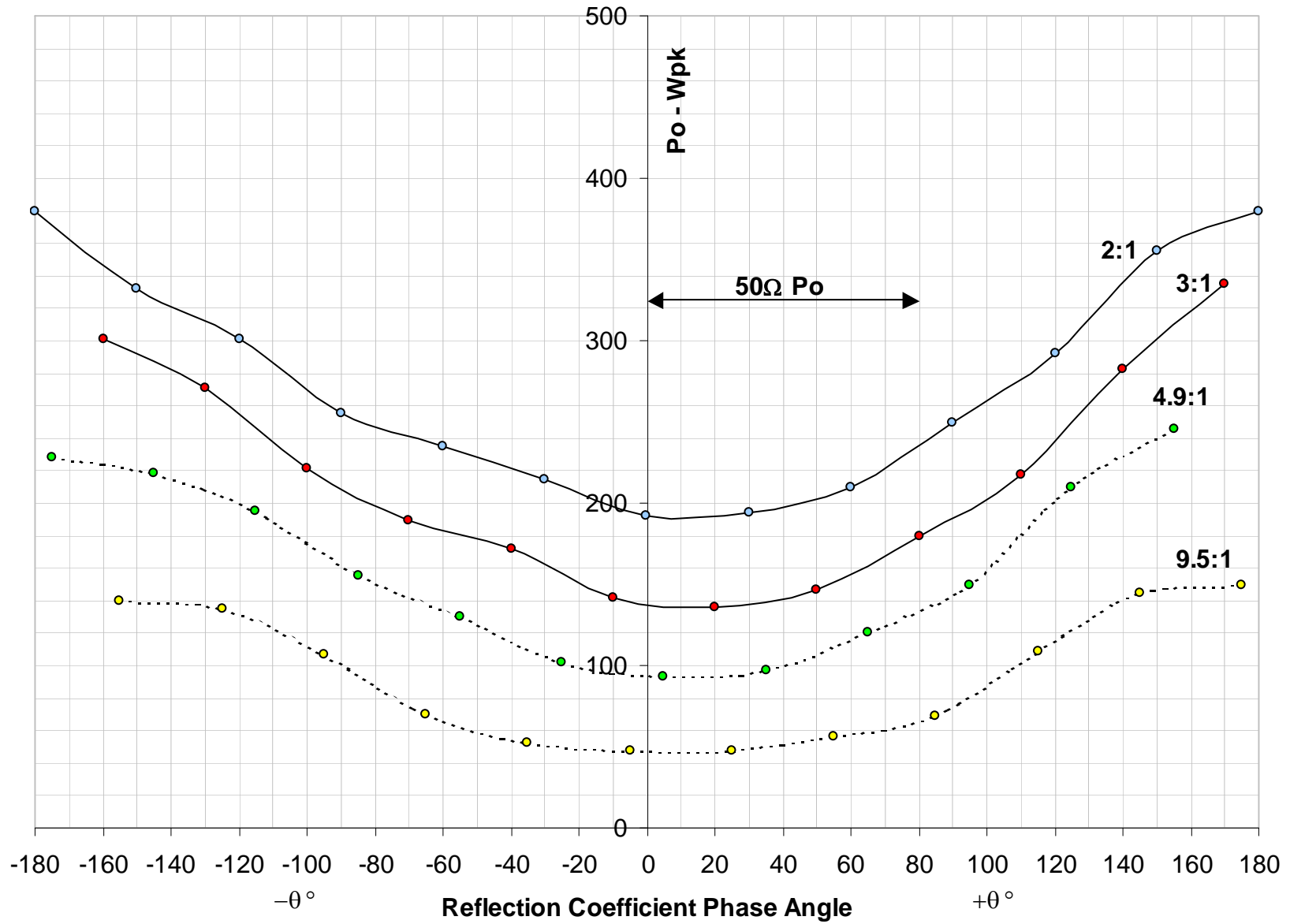
Figure 6



45 MHz Test Model VSWR Performance

B+ = 48V, PW = 200 μ sec, Duty Cycle = 10%

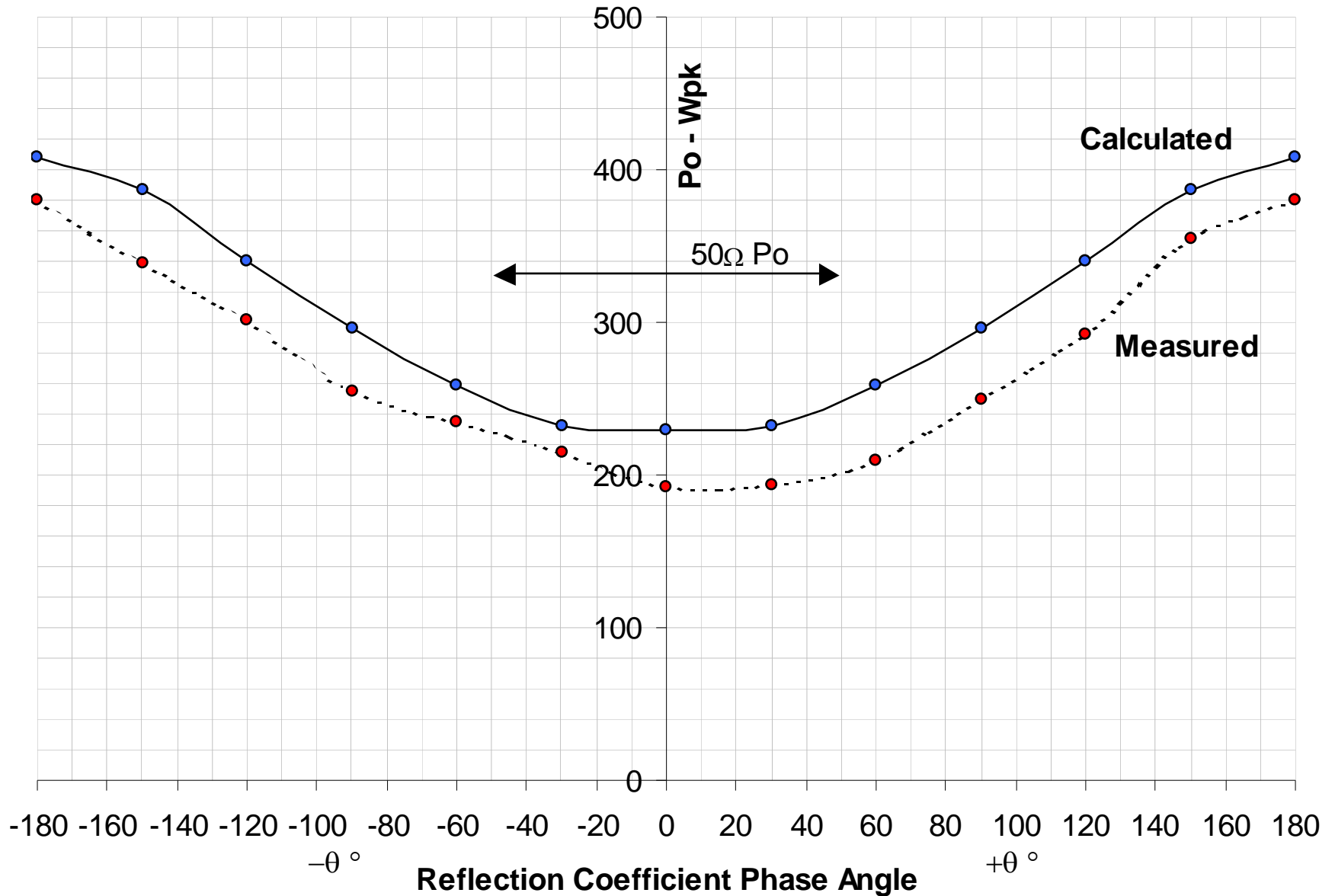
Figure 7



Po vs. θ for Calculated and Measured Performance

$R_S = 20\Omega$ for calculated data, $B_+ = 48V$, $f_o = 45$ MHz for Test RFPA

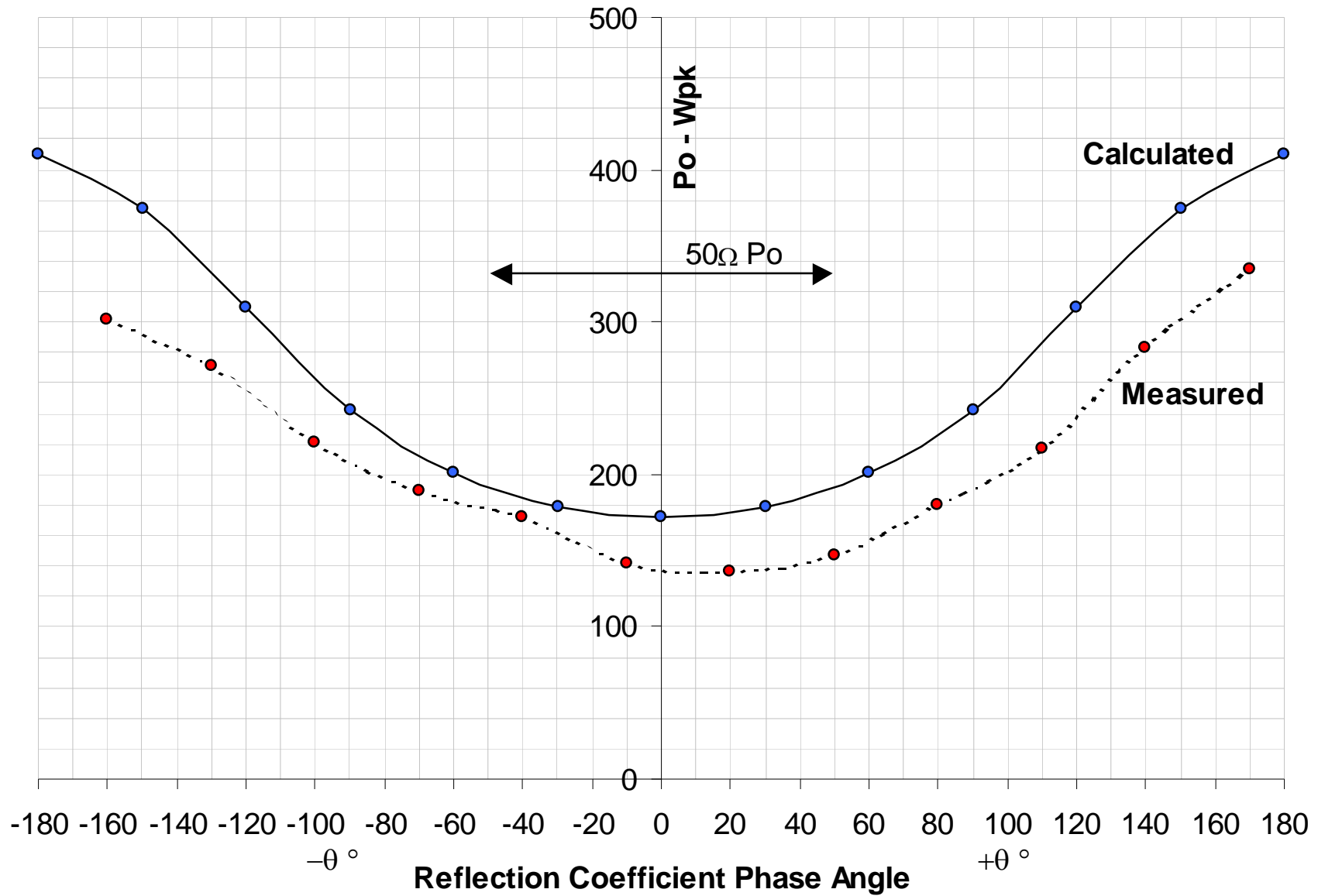
Figure 8 VSWR = 2:1



Po vs. θ for Calculated and Measured Performance

$R_S = 20\Omega$ for calculated data, $B_+ = 48V$, $f_o = 45$ MHz for Test RFPA

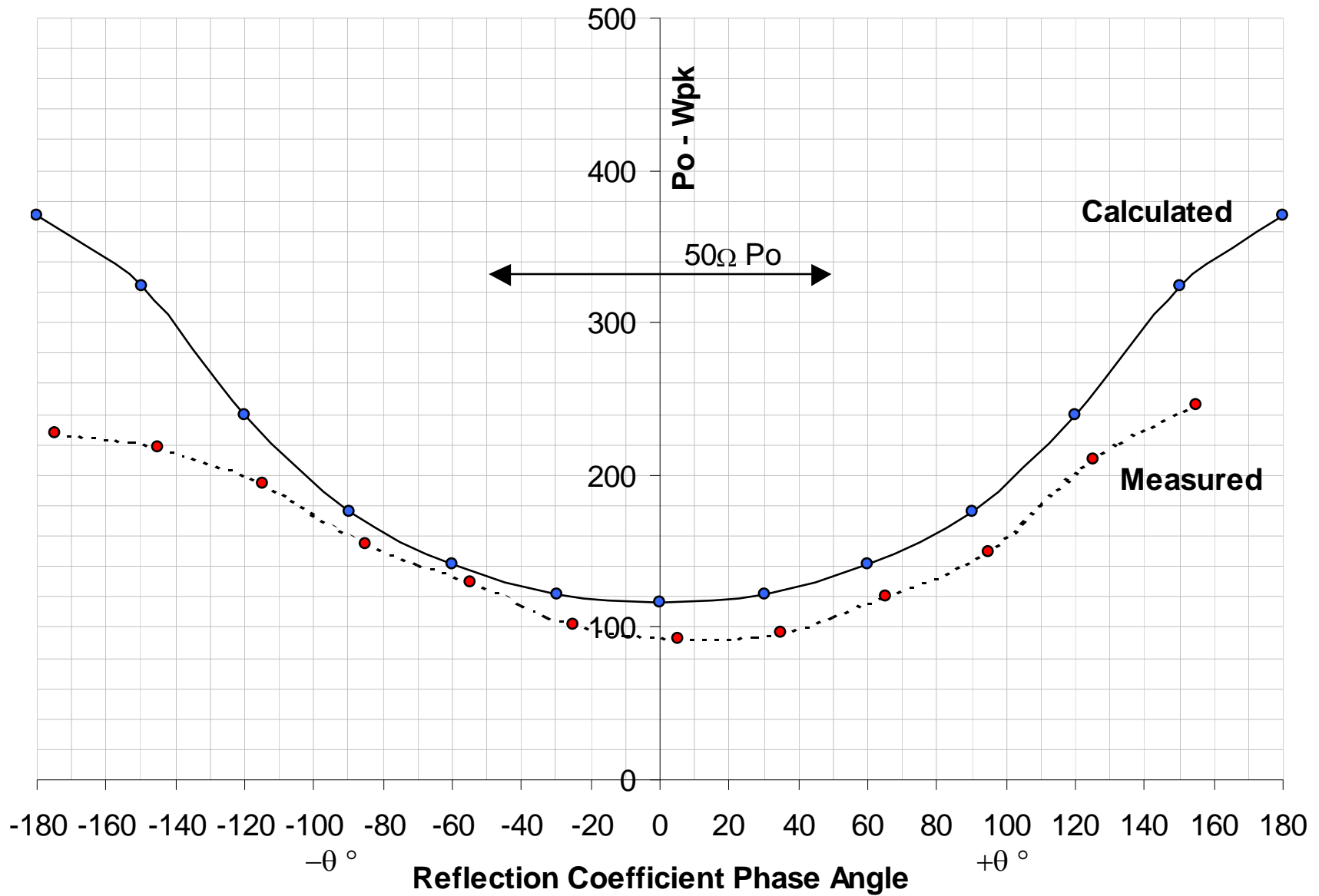
Figure 9 VSWR = 3:1



Po vs. θ for Calculated and Measured Performance

$R_S = 20\Omega$ for calculated data, $B_+ = 48V$, $f_o = 45$ MHz for Test RFPA

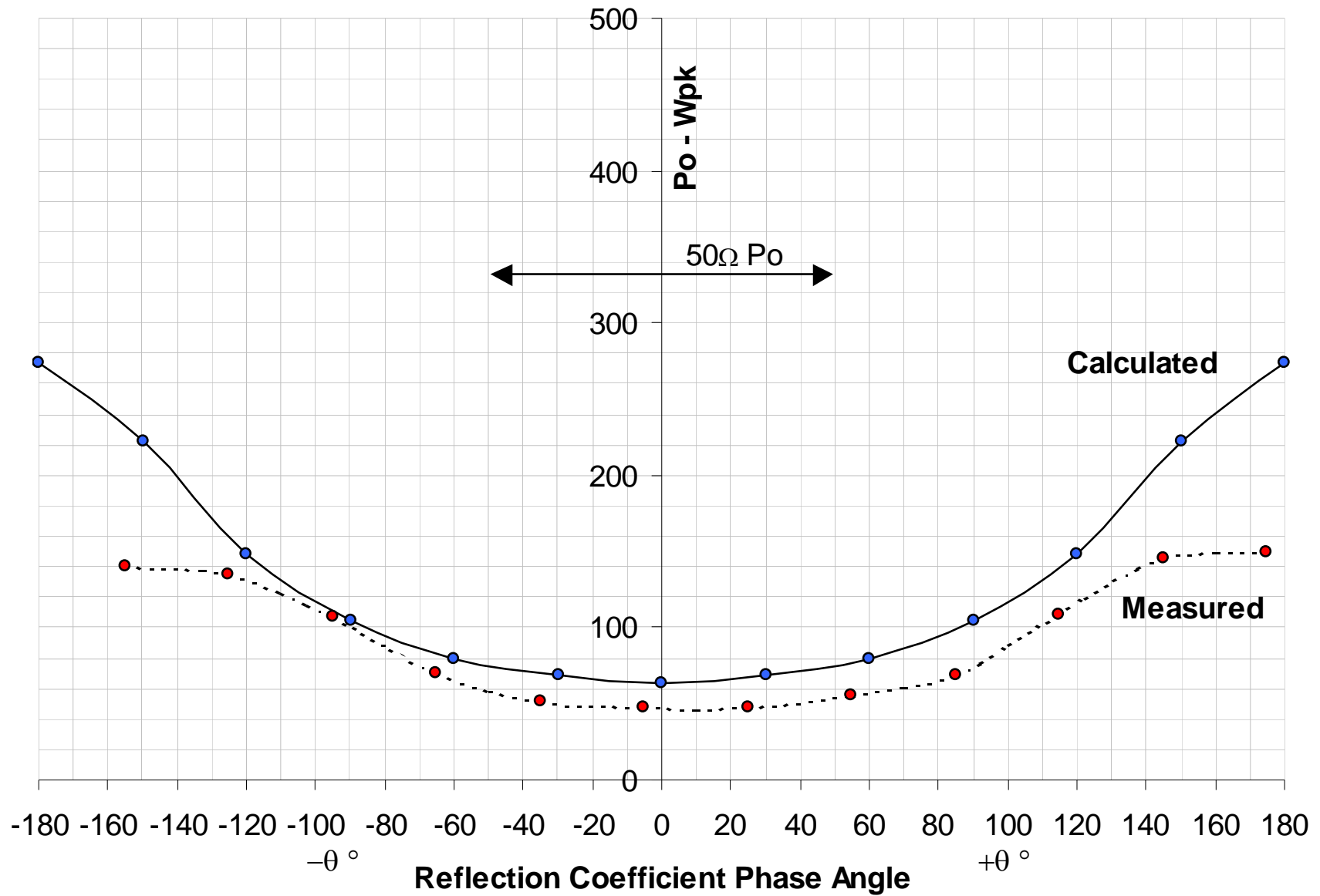
Figure 10 VSWR = 4.9:1



Po vs. θ for Calculated and Measured Performance

$R_S = 20\Omega$ for calculated data, $B_+ = 48V$, $f_o = 45$ MHz for Test RFPA

Figure 11 VSWR = 9.5:1



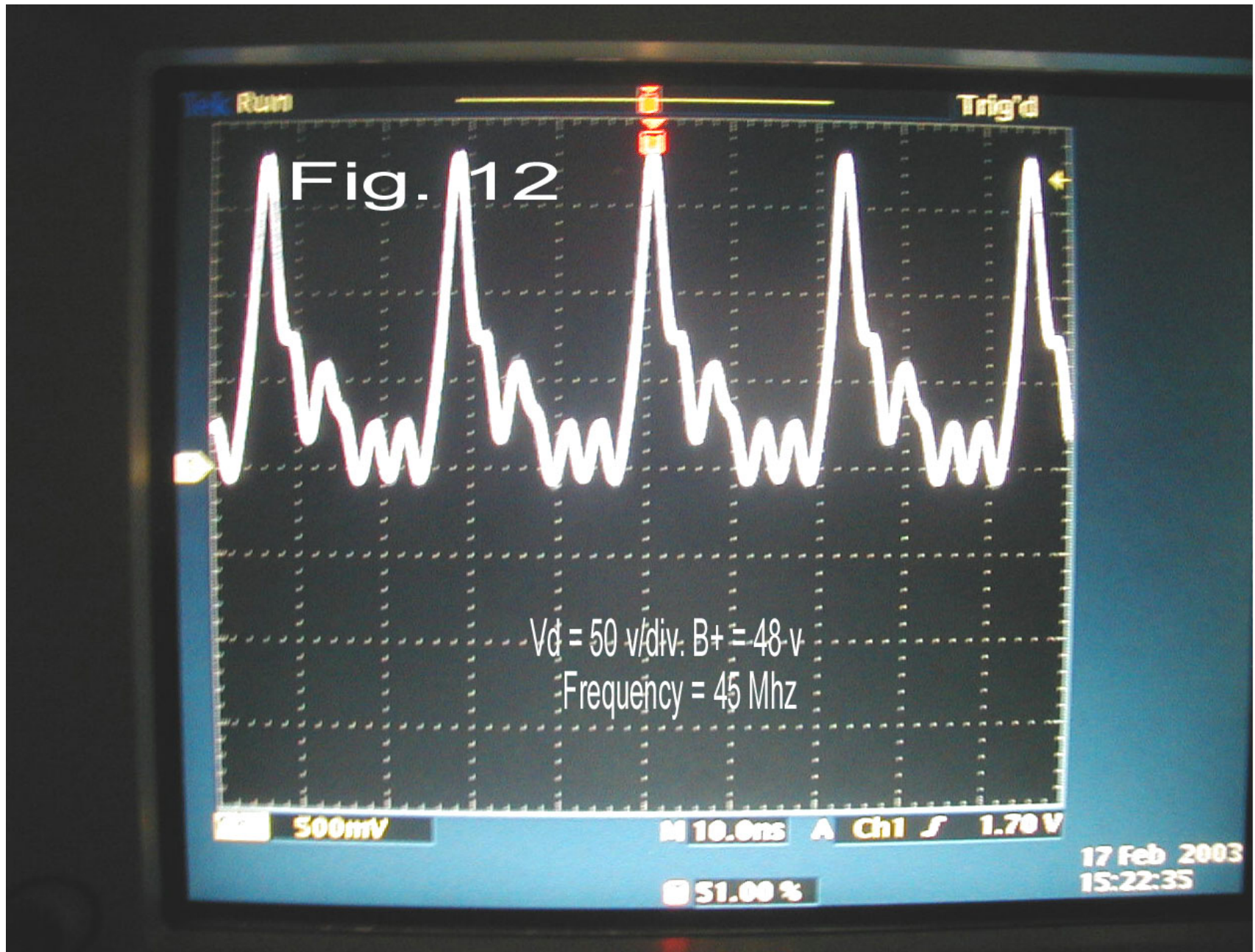
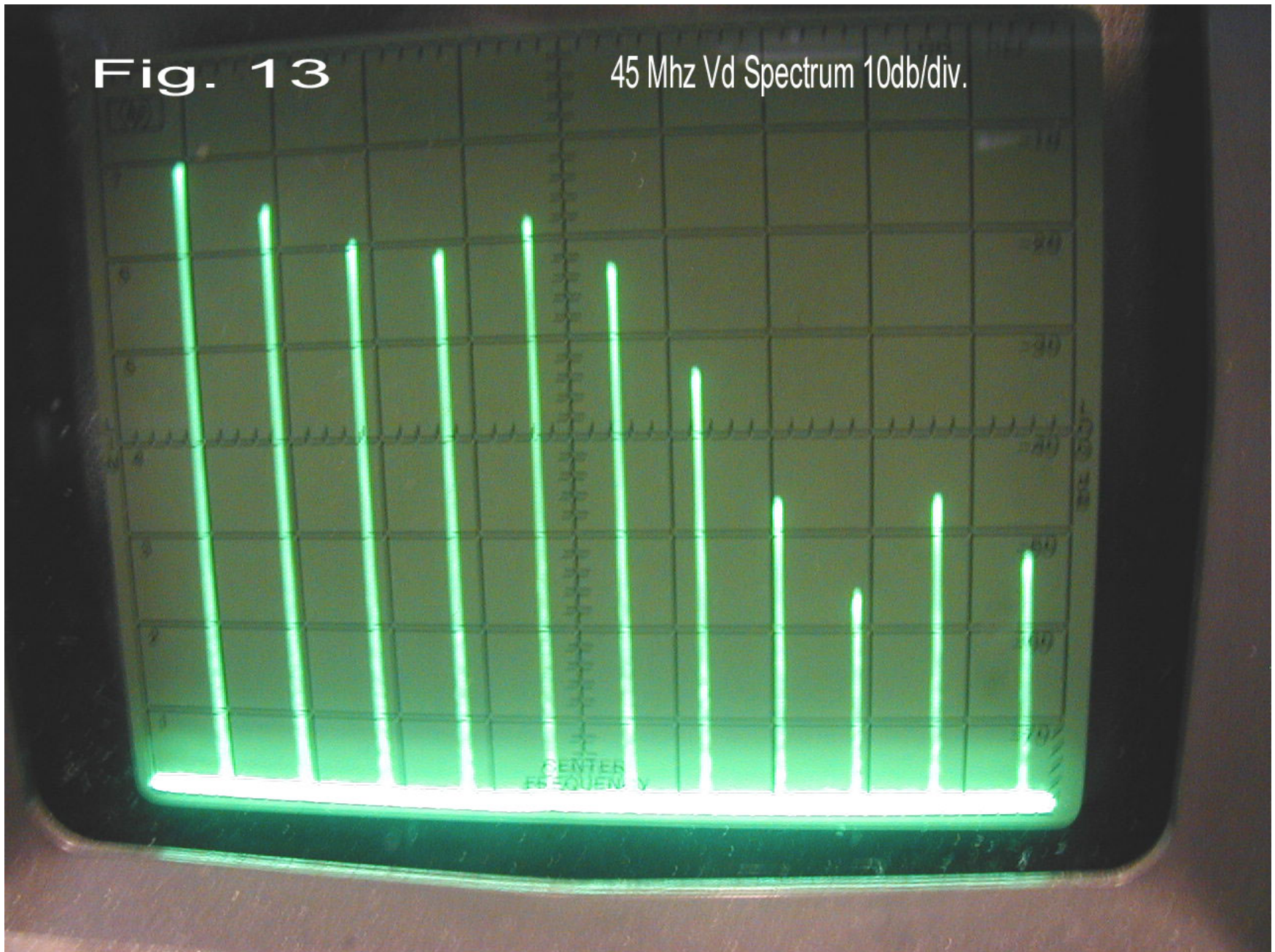
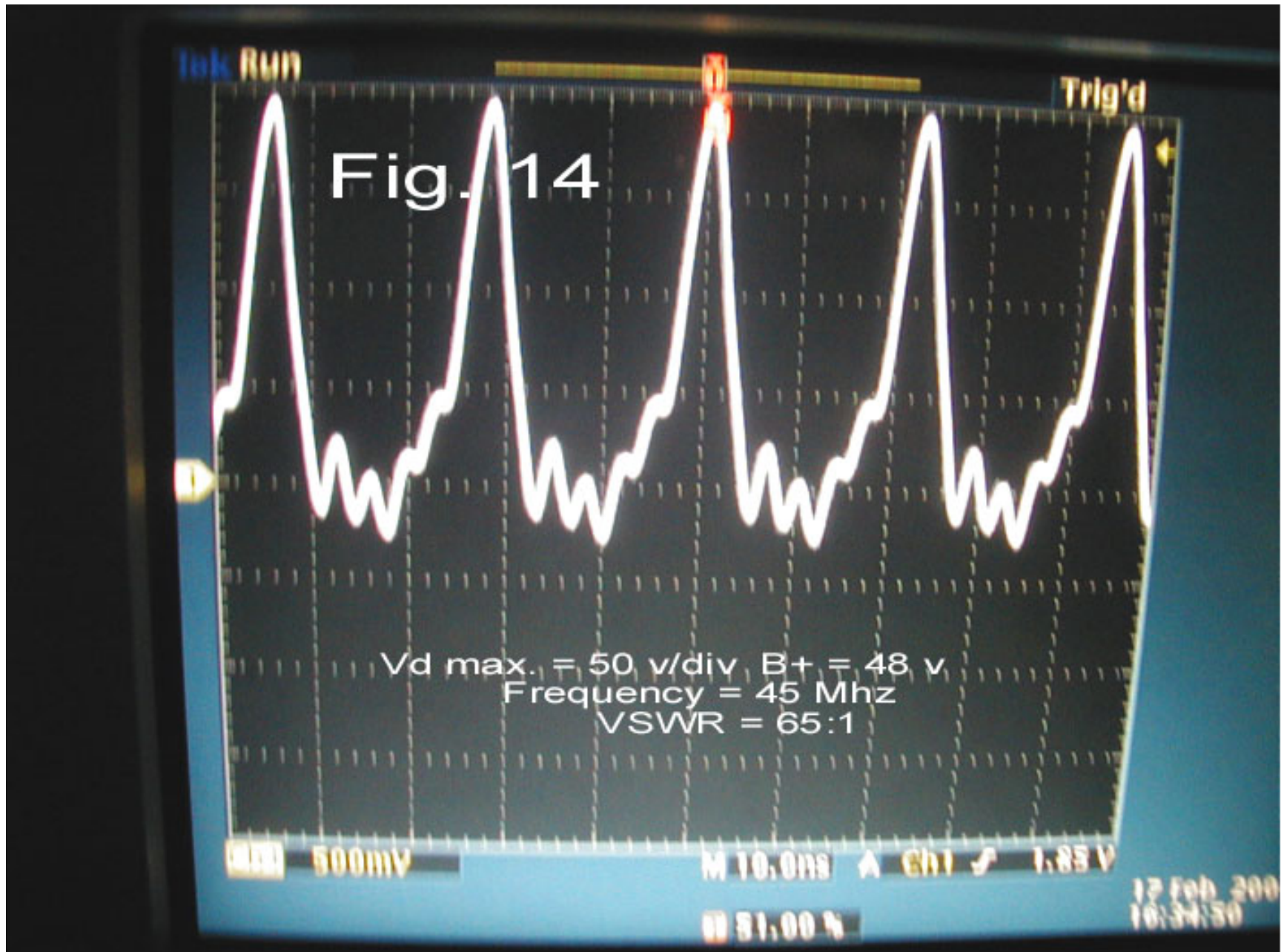


Fig. 13

45 Mhz Vd Spectrum 10db/div.



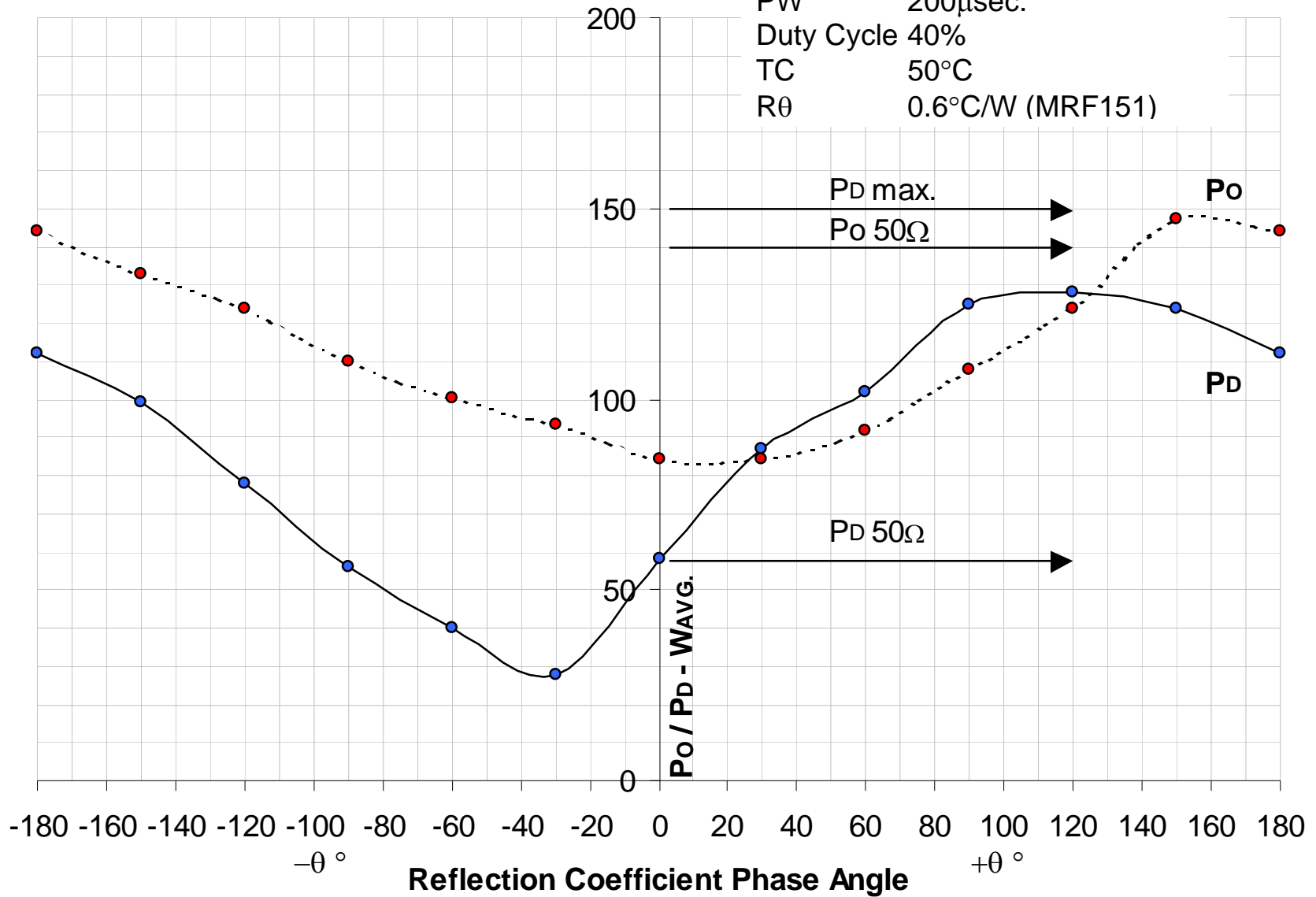


Power Output and Power Dissipated vs. θ for VSWR = 2:1

Figure 15

Conditions

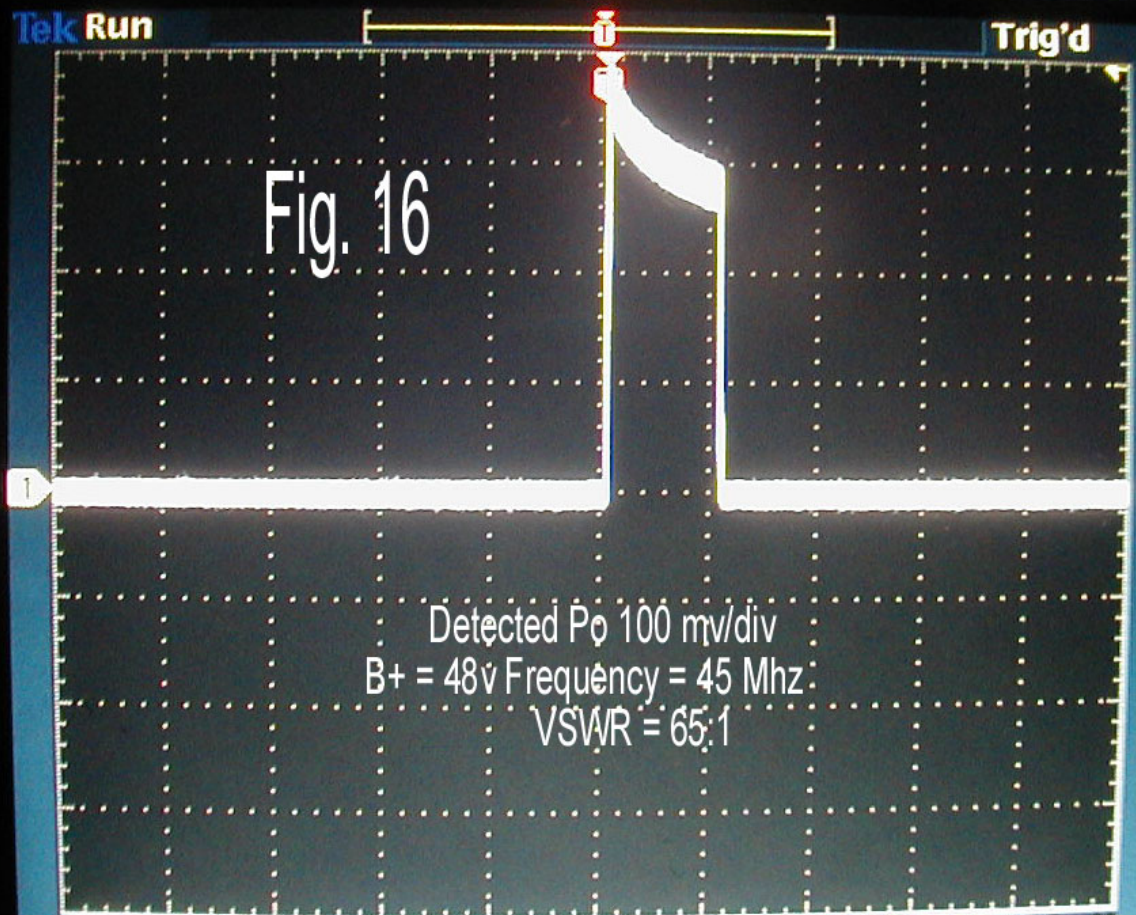
Frequency 45 MHz
B+ 48V
PW 200 μ sec.
Duty Cycle 40%
TC 50°C
R θ 0.6°C/W (MRF151)



Tek Run

Trig'd

Fig. 16



Detected P₀ 100 mV/div
B+ = 48V Frequency = 45 Mhz
VSWR = 65:1

Ch1 100mV

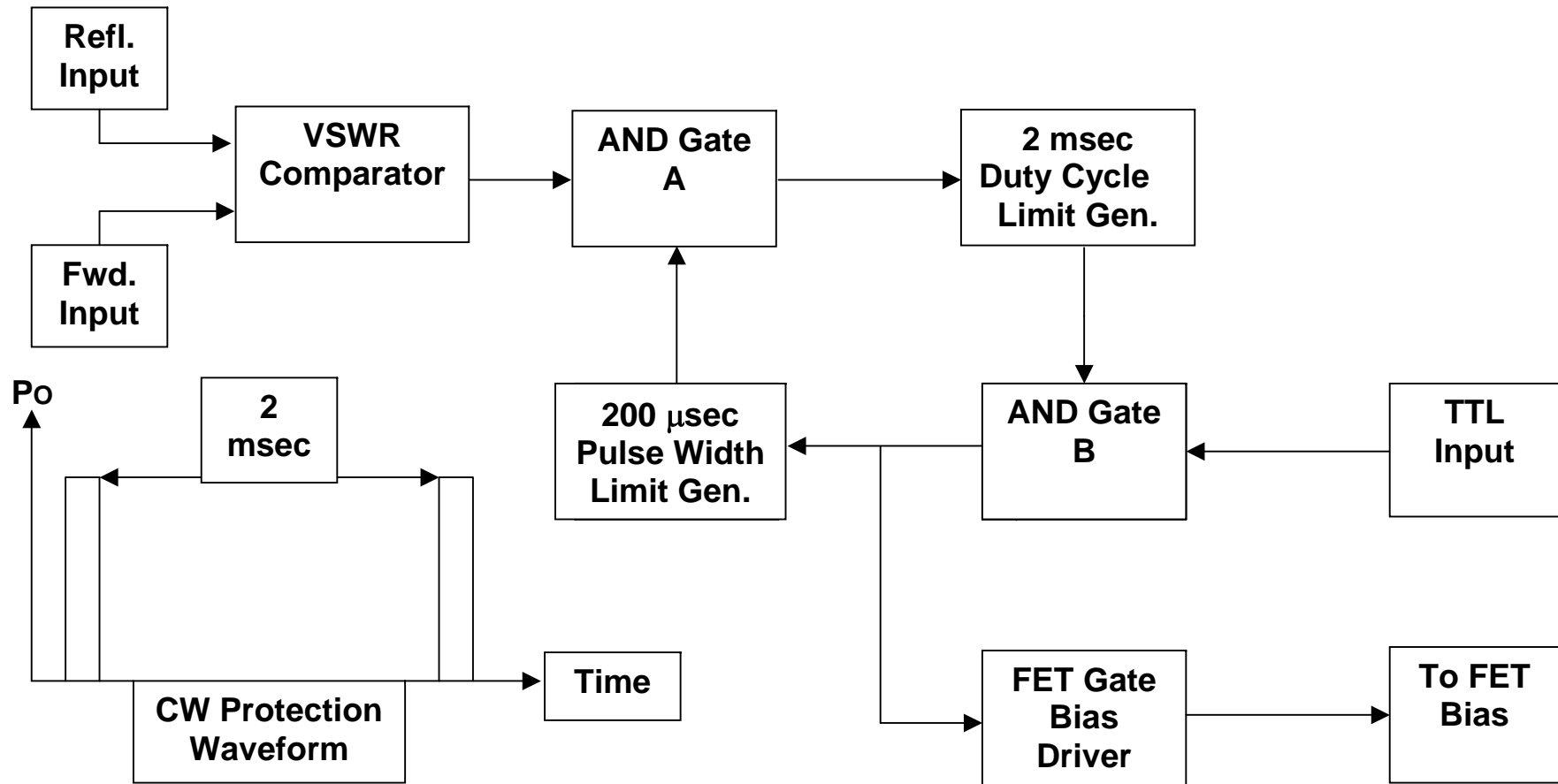
M 200µs A Ch1 398mV

51.00%

17 Feb 2003
17:01:29

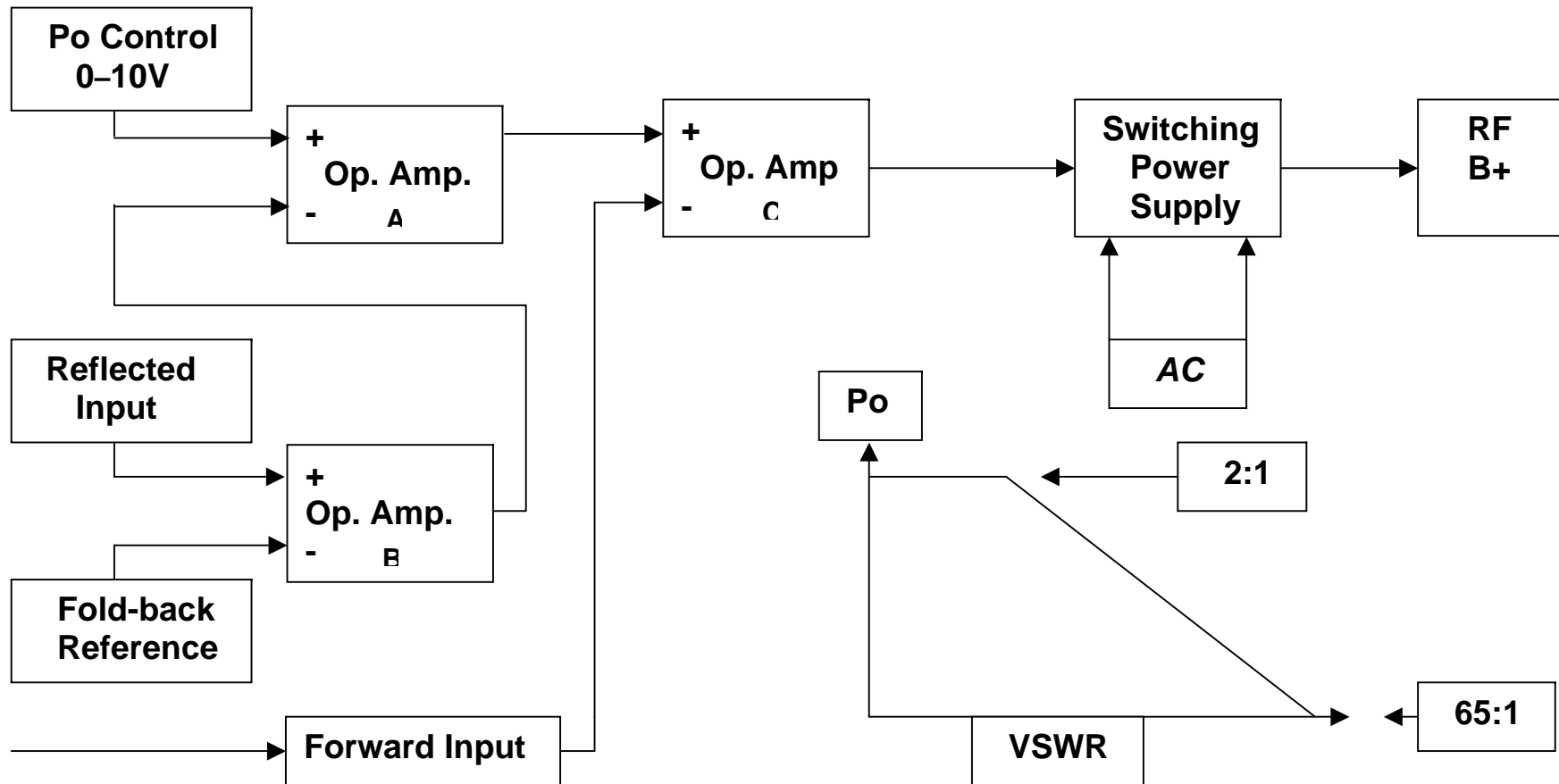
Basic Pulse Width and Duty Cycle Limit VSWR Protection Block Diagram

Figure 17



Basic Foldback VSWR Protection and Feedback Control Block Diagram

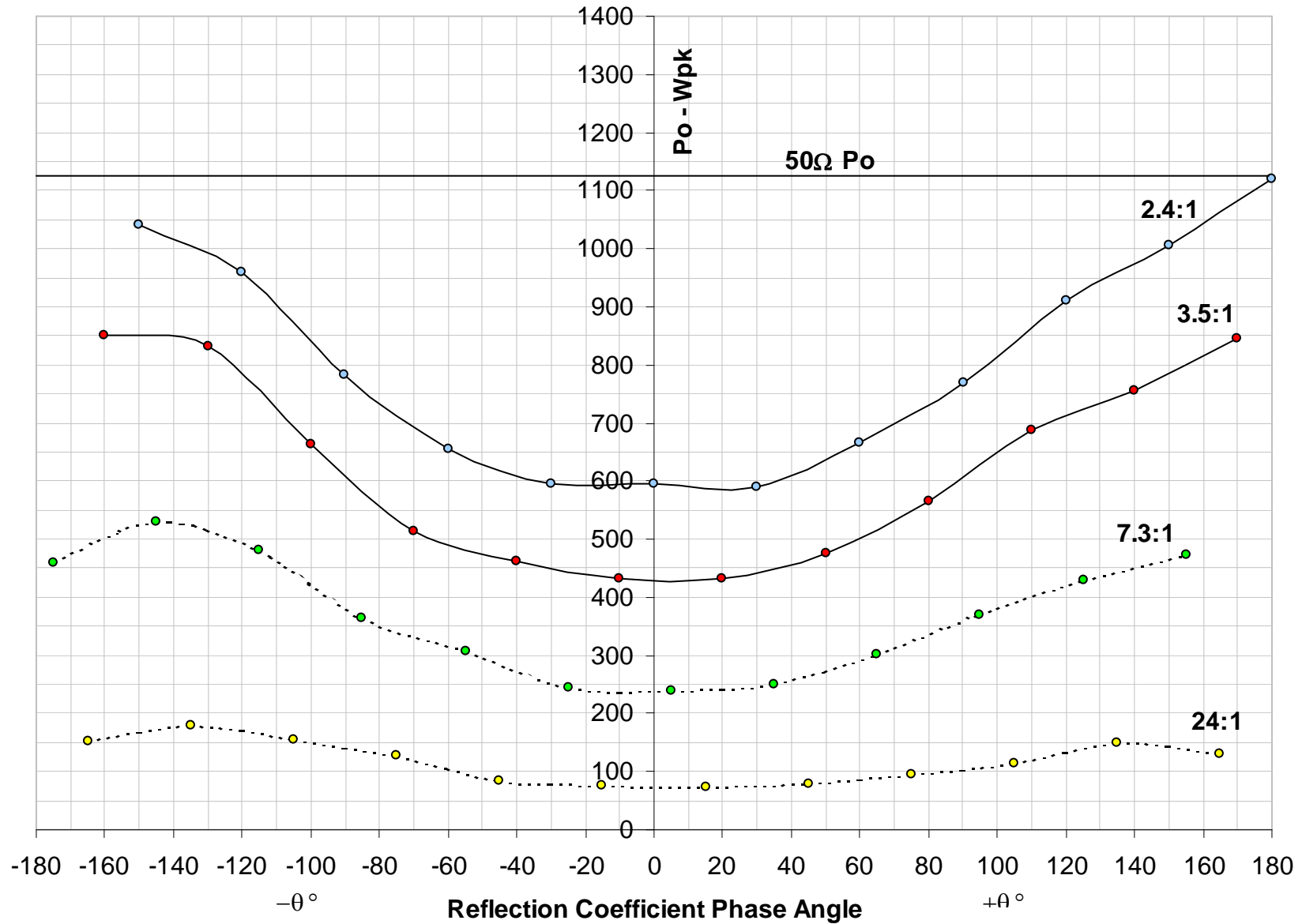
Figure 18



4 Transistor RFPA Laser Driver VSWR Performance

B+ = 48V

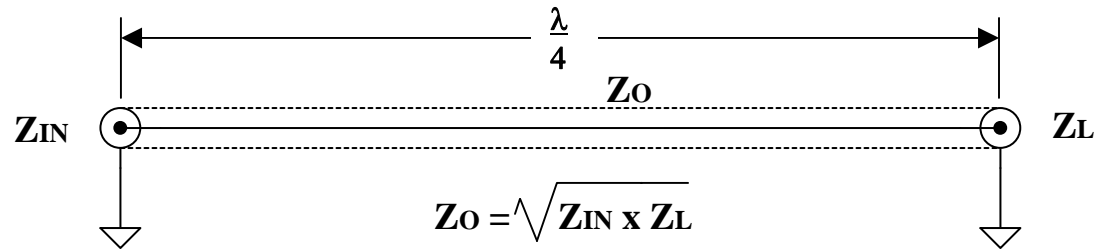
Figure 20



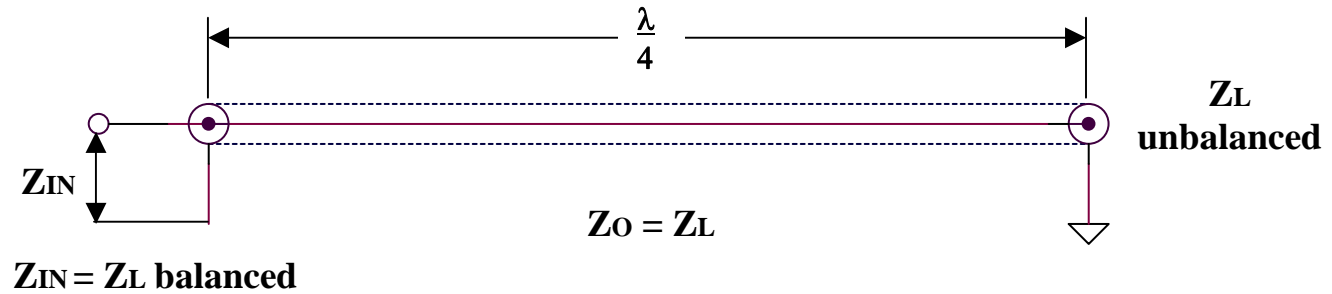
Transmission Line Matching

Figure 21A

1. Quarter – Wave Transmission Line



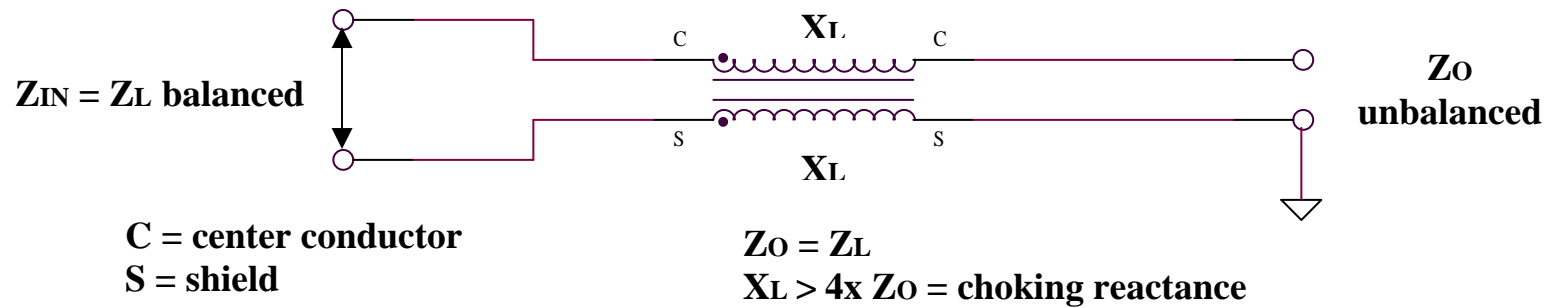
2. Quarter – Wave Balun



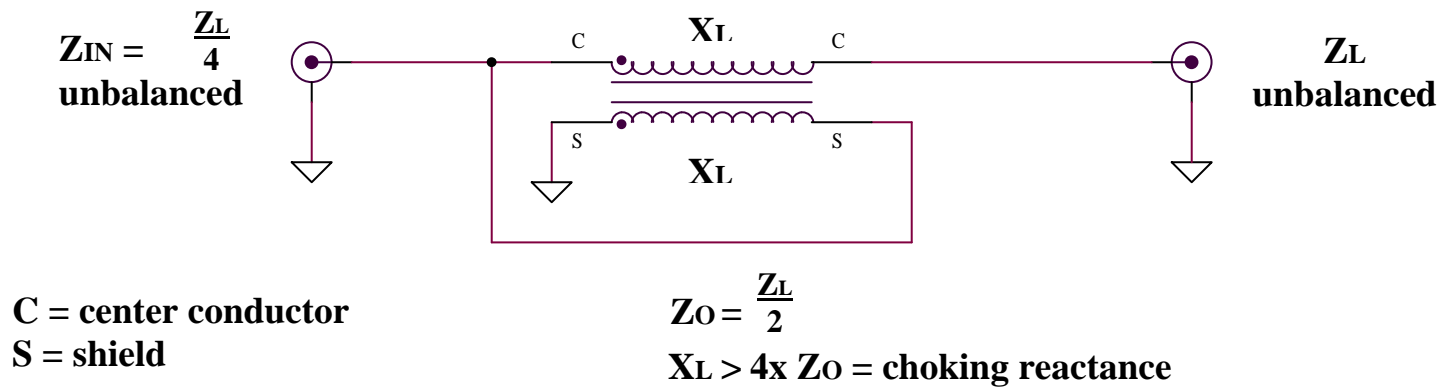
Transmission Line Matching

Figure 21B

1. Ferrite Loaded Balun



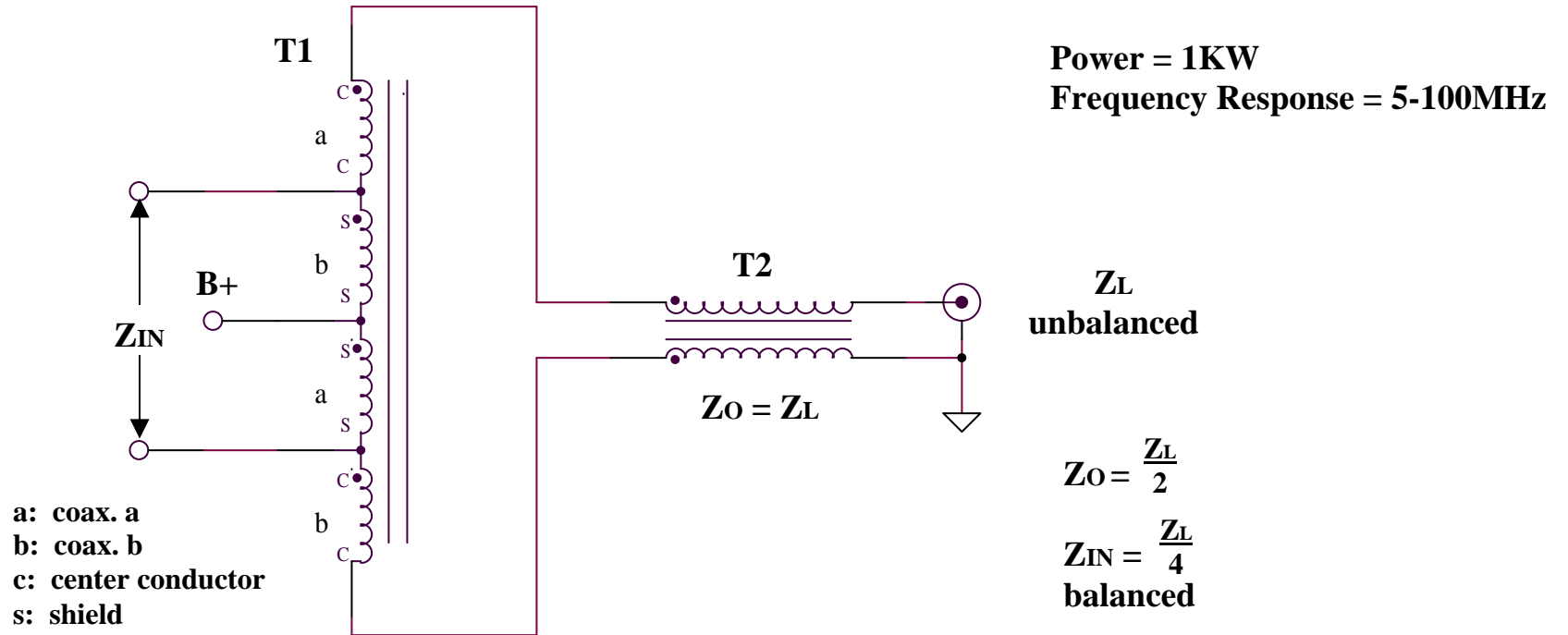
2. 4:1 Ferrite Loaded Unun



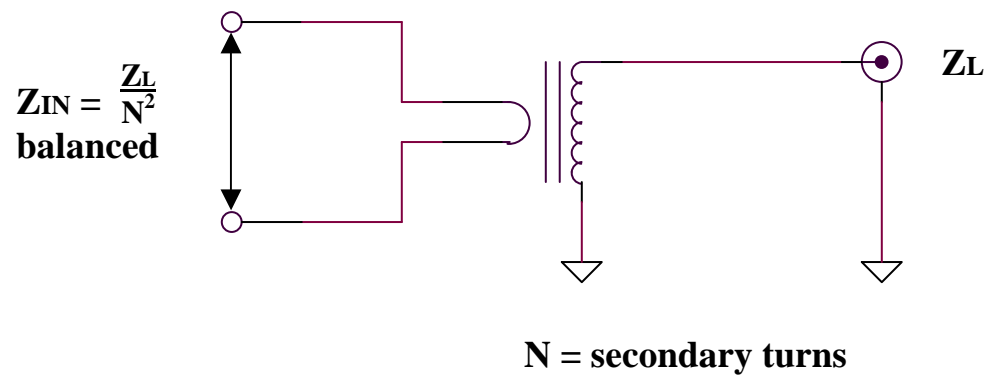
Transmission Line Matching

Figure 21C

1. 4:1 Ferrite Loaded High Power Balun



2. Single Turn Primary Tube Transformer

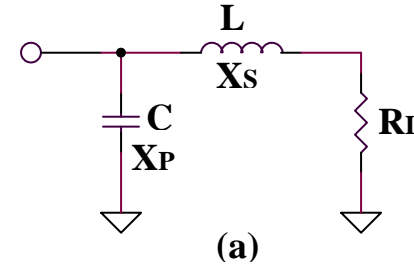


LC Matching Circuits

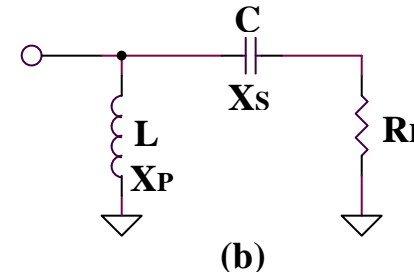
Figure 22A

1. $R_{IN} > R_L$

$$X_S = R_L \sqrt{\frac{R_{IN}}{R_L} - 1}$$

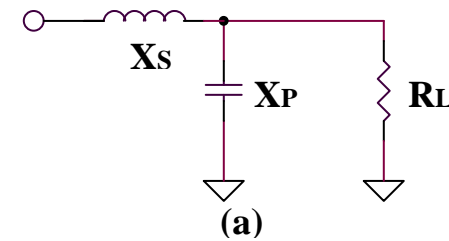


$$X_P = X_S \left(\frac{\left(\frac{X_S}{R_L}\right)^2 + 1}{\left(\frac{X_S}{R_L}\right)^2} \right)$$



2. $R_{IN} < R_L$

$$X_P = \frac{R_L}{\sqrt{\frac{R_L}{R_{IN}} - 1}}$$



$$X_S = X_P \left(\frac{\left(\frac{R_L}{X_P}\right)^2}{\left(\frac{R_L}{X_P}\right)^2 + 1} \right)$$

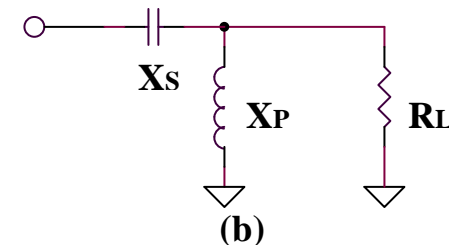
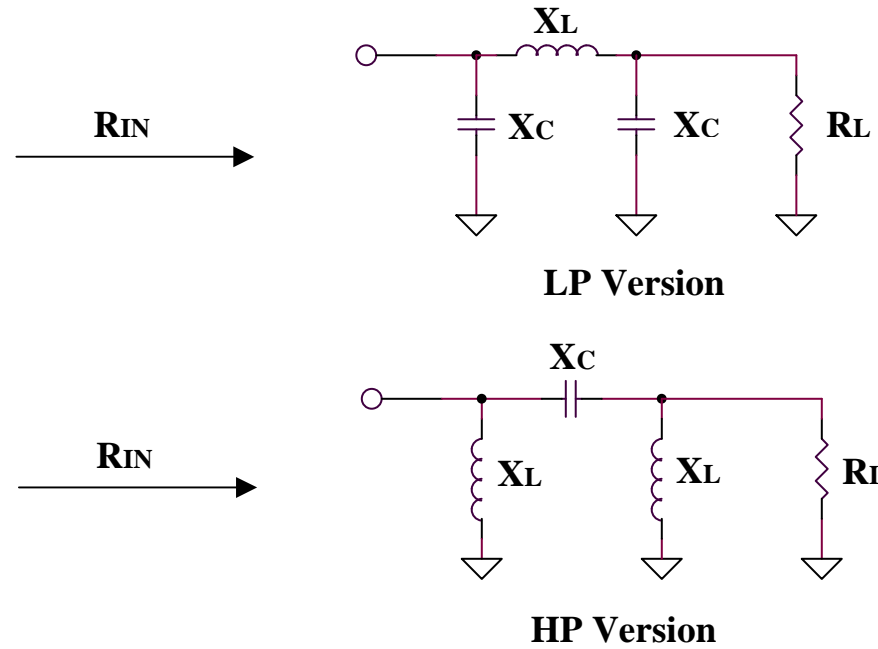


Figure 22B

1. $R_{IN} > \text{or} < R_L$

$$X_C = X_L = \sqrt{R_{IN} \times R_L}$$

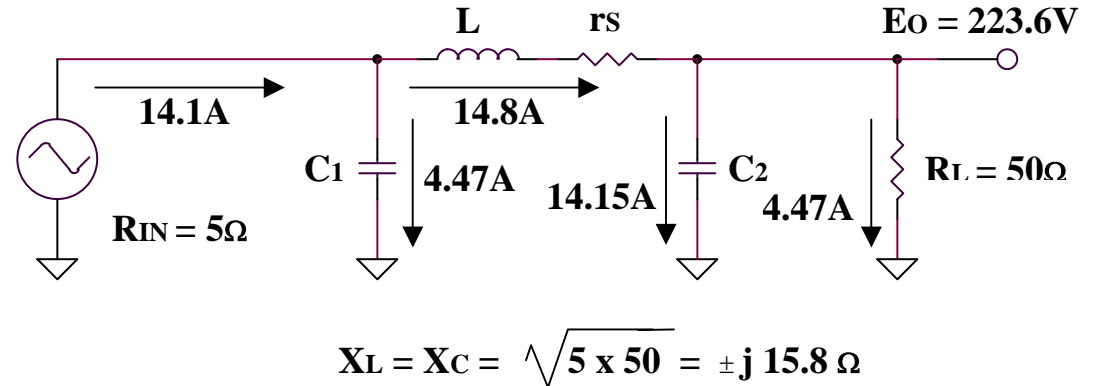
π Match



2. High Power π Match Design

Performance

P_o	1KW
Frequency	80MHz
$R_L \div R_{IN}$	10:1
Q_L	250, $r_s = .06\Omega$ $P_D (r_s) = 13W$
C_1	126pF ATC100E
C_2	2 x 63pF ATC100E
L	31nH



High Power Pin Diode Switch

Figure 23

